CLAIMS

1. A semiconductor device comprising:

a substrate including an n-type first single-crystal semiconductor layer functioning as a collector layer;

a p-type second single-crystal semiconductor layer formed on the first single-crystal semiconductor layer, the second single-crystal semiconductor layer containing a p-type impurity and functioning as a base layer;

a third single-crystal semiconductor layer formed on the second single-crystal semiconductor layer, an upper portion of the third single-crystal semiconductor layer containing phosphorus in a concentration equal to or less than the solid-solubility limit, at least part of the third single-crystal semiconductor layer functioning as an emitter; and

an emitter lead electrode formed on the third single-crystal semiconductor layer, the emitter lead electrode being made of a semiconductor layer containing phosphorus in a concentration higher than that in the upper portion of the third single-crystal semiconductor layer.

2. A semiconductor device comprising:

a substrate including an n-type first single-crystal semiconductor layer functioning as a collector layer;

a p-type second single-crystal semiconductor layer formed on the first single-crystal semiconductor layer, the

second single-crystal semiconductor layer containing a p-type impurity and functioning as a base layer; and

a third single-crystal semiconductor layer formed on the second single-crystal semiconductor layer, at least an upper portion of the third single-crystal semiconductor layer containing a p-type impurity and phosphorus in a concentration higher than the concentration of the p-type impurity, at least part of the third single-crystal semiconductor layer functioning as an emitter.

3. The semiconductor device of Claim 2, wherein the concentration of the p-type impurity in the upper portion of the third single-crystal semiconductor layer is equal to or higher than the concentration of the p-type impurity in the second single-crystal semiconductor layer.

4. The semiconductor device of Claim 2 or 3, wherein the first single-crystal semiconductor layer is a Si layer, the second single-crystal semiconductor layer is a SiGe layer, and the third single-crystal semiconductor layer is a Si layer.

5. The semiconductor device of Claim 2 or 3, wherein the first single-crystal semiconductor layer is a Si layer, the second single-crystal semiconductor layer is a SiGeC layer,

and the third single-crystal semiconductor layer is a Si layer.

6. A method for fabricating a semiconductor device, comprising the steps of:

(a) epitaxially growing a p-type second single-crystal semiconductor layer functioning as a base layer on an n-type first single-crystal semiconductor layer functioning as a collector layer on a substrate;

(b) epitaxially growing a third single-crystal semiconductor layer on the second single-crystal semiconductor layer;

(c) depositing a semiconductor layer on the third single-crystal semiconductor layer, the semiconductor layer including a bottom portion containing phosphorus in a concentration equal to or lower than a concentration permitting phosphorus to be diffused into the third single-crystal semiconductor layer in a concentration as high as the solid-solubility limit for the third single-crystal semiconductor layer, and an upper portion containing phosphorus in a concentration higher than that in the bottom portion; and

(d) performing heat treatment for diffusing phosphorus in the semiconductor layer so that the upper portion of the third single-crystal semiconductor layer is doped with

phosphorus in a concentration equal to or lower than the solid-solubility limit, to form an emitter of a bipolar transistor.

7. The method for fabricating a semiconductor device of Claim 6, wherein in the step (c), the concentration of phosphorus introduced into the semiconductor layer is increased in stages toward the upper portion.

8. The method for fabricating a semiconductor device of Claim 6, wherein in the step (c), the concentration of phosphorus introduced into the semiconductor layer is increased sequentially toward the upper portion.

9. The method for fabricating a semiconductor device of any one of Claims 6 to 8, wherein in the step (a), a SiGe layer as the second single-crystal semiconductor layer is epitaxially grown on a Si layer as the first single-crystal semiconductor layer, and

in the step (b), a Si layer as the third single-crystal semiconductor layer is epitaxially grown.

10. The method for fabricating a semiconductor device of any one of claims 6 to 8, wherein in the step (a), a SiGeC layer as the second single-crystal semiconductor layer is

epitaxially grown on a Si layer as the first single-crystal semiconductor layer, and

in the step (b), a Si layer as the third single-crystal semiconductor layer is epitaxially grown.

11. A method for fabricating a semiconductor device, comprising the steps of:

(a) epitaxially growing a p-type second single-crystal semiconductor layer functioning as a base layer on an n-type first single-crystal semiconductor layer functioning as a collector layer on a substrate;

(b) epitaxially growing a third single-crystal semiconductor layer on the second single-crystal semiconductor layer;

(c) doping at least an upper portion of the third single-crystal semiconductor layer with a p-type impurity;

(d) forming a semiconductor layer containing phosphorus on the third single-crystal semiconductor layer; and

(e) performing heat treatment for diffusing phosphorus in the semiconductor layer so that the upper portion of the third single-crystal semiconductor layer is doped with phosphorus in a concentration higher than the concentration of the p-type impurity introduced in the step (c), to form an emitter of a bipolar transistor.

12. The method for fabricating a semiconductor device of Claim 11, wherein the step (c) is performed simultaneously with the step (b) by epitaxially growing the third single-crystal semiconductor layer while being doped with the p-type impurity.

13. The method for fabricating a semiconductor device of Claim 11, wherein the step (c) is performed after the step (b) by implanting ions of the p-type impurity in the third single-crystal semiconductor layer.

14. The method for fabricating a semiconductor device of claim 11, further comprising the steps of:

forming an insulating layer on the third single-crystal semiconductor layer after the step (b) and before the step (c); and

forming a semiconductor layer containing a p-type *impurity on the insulating layer,*

wherein the step (c) is performed by introducing the p-type impurity into the third single-crystal semiconductor layer from the semiconductor layer via the insulating layer.